

## Claims

What is claimed is:

1. A method of checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the  
5 method comprising the steps of:

for a given clock cycle, detecting the presence of an error bit in the output PRBS,  
the error bit representing a mismatch between the input PRBS and the output PRBS; and  
prohibiting propagation of the error bit for subsequent clock cycles.

10 2. The method of claim 1, wherein the prohibition step serves to avoid at least  
one of multiple errors being counted for a single error occurrence and masking errors in  
the output PRBS.

15 3. The method of claim 1, wherein the prohibition step further comprises  
correcting the error bit.

4. The method of claim 1, further comprising the step of detecting the  
non-presence of a PRBS from the device.  
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5. The method of claim 1, wherein the device is one of a communication circuit  
and a communication channel.

20 6. Apparatus for checking the accuracy of an output pseudorandom bit sequence  
(PRBS) generated by a device in response to an input PRBS received by the device, the  
apparatus comprising:

a memory; and

at least one processor coupled to the memory and operative to: (i) for a given clock cycle, detect the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and (ii) prohibit propagation of the error bit for subsequent clock cycles.

5        7. The apparatus of claim 6, wherein the prohibition operation serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the output PRBS.

8. The apparatus of claim 6, wherein the prohibition operation further comprises correcting the error bit.

10      9. The apparatus of claim 6, wherein the at least one processor is further operative to detect the non-presence of a PRBS from the device.

10. The apparatus of claim 6, wherein the device is one of a communication circuit and a communication channel.

15      11. An article of manufacture for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, comprising a machine readable medium containing one or more programs which when executed implement the steps of:

for a given clock cycle, detecting the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and  
20      prohibiting propagation of the error bit for subsequent clock cycles.

12. Apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising:

- a shift register chain;
- 5 a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and
- 10 at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

13. The apparatus of claim 12, further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain.

14. The apparatus of claim 13, wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector.

15. The apparatus of claim 12, further comprising an error counter coupled to the logic gate for counting errors detected between the input PRBS and the output PRBS.

20 16. The apparatus of claim 15, further comprising an error count display coupled to the error counter for displaying the error count.

17. The apparatus of claim 12, further comprising a third logic detector coupled to the shift register chain for detecting the non-presence of a PRBS from the device.